REMARKS

The Examiner's action mailed on December 13, 2001 has been received and its contents carefully considered.

Claims 20, 22 and 24-29 are pending in this application. Claim 28 is amended and new claims 30-31 are added herein. Claims 20, 26 and 28 are independent claims.

The changes to claim 28 are shown in Appendix 1 to this Amendment with deletions indicated by bracketing and additions by underlining.

Claims 20, 22, 24 and 28 stand rejected under 35 USC 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or using the invention. Specifically, the Examiner asserts that in neither the description nor the original set of claims has the applicant mentioned that the pitch, or distance, between the connection solder bumps is less than the intermediate distance between the central solder bump area and the peripheral solder bump area.

It is respectfully submitted, contrary to the Examiner's position, that support for this claimed feature can be found in the figures, which are also considered to be part of the disclosure of the original application. Figure 2, in particular, clearly discloses that the back surface 11a of the semiconductor device has a central area in which a first plurality of bumps 13 are disposed a first distance apart from each other, an intermediate area surrounding the central area, in which no bumps are disposed, and a peripheral area, surrounding the intermediate area, in which a second plurality of bumps 14 are disposed a second distance apart from each other. In addition to disclosing an intermediate area, as

claimed, Figure 2 and the other figures show that the width of the intermediate area (i.e., the distance between the central area and a peripheral area) is greater than the distance between the individual bumps 14 of the second bump unit.

To provide support for the rejected claims, the specification is amended herein to recite the features discussed above. Inasmuch as these features are already disclosed in the original figures submitted as part of the application, it is respectfully submitted that the amendments herein to the specification do not constitute new matter. Accordingly, it is requested that the amendments to the specification be entered and that the §112, first paragraph, rejection be withdrawn.

The changes to the specification are shown in Appendix 2 to this Amendment with deletions indicated by bracketing and additions by underlining.

Claims 20, 22 and 24-29 stand rejected under 35 USC §103(a) as being obvious over *Katchmar* (U.S. Patent No. 6,194,782 B1). The rejection is respectfully traversed.

In the Action, the Examiner asserts that Katchmar teaches a semiconductor device, Figures 1-5, comprising: a substrate 12 having a main surface 14 and a back surface 16, wherein said back surface 16 has a central area 32, an intermediate area surrounding said central area 32 and a peripheral area surrounding said intermediate area; a semiconductor chip 18 formed on said main surface; a first bump unit formed of solder bumps 40, Figure 5, and located in said central area of said back surface, wherein said first bump unit radiates heat from said semiconductor device; a second bump unit formed of solder bumps 24 and located in said peripheral area of said back surface, wherein said second bump unit transmits signals (column 6, lines 50-53), wherein the second bump unit is greater in

quantity of solder balls than the first bump unit, and said solder balls are spherical in shape. Furthermore, the Examiner asserts that Katchmar teaches a first distance between connection solder balls being greater than a second distance between heat transfer solder balls (column 7, lines 39-47).

Contrary to the Examiner's assertions, it is respectfully submitted that Katchmar fails to teach or suggest a distinct intermediate area between the central area and the peripheral area, as required by the rejected claims. What Figures 1-4 disclose, for example, is a ball grid array with uniform spacing in which the solder mass 26 replaces the solder balls in the area under the semiconductor chip 18, and only in that area, and the remainder of the bottom surface 16 of the substrate 12 is available for placement of solder balls (column 6, line 66, through column 7, line 3). In Figure 5 of Katchmar, a plurality of closely spaced solder balls 40 replaces the single solder mass 26 under the semiconductor chip (column 7, lines 39-48). However, unlike the present invention, none of the embodiments described in Katchmar involve an intermediate area, marked by a lack of solder balls, between the central area and the peripheral area.

The Examiner's Action also fails to demonstrate that Katchmar teaches or suggests the limitation recited in the rejected claims that "said second distance (between the bumps of the second bump unit) is less than a third distance between said central area and said peripheral area." Regarding this limitation, the Examiner argues that the applicant has not shown that this particular range is critical by showing that the claimed range achieves unexpected results relative to the prior art range. First, as noted above, there is no prior art range because Katchmar fails to disclose any intermediate area at all, let alone the relative

size of such an intermediate area. Further, it is submitted that that the standards and tests applied by the Examiner are not applicable to the present case. The invention claimed in claims 20, 26 and 28 are not directed to specific ranges of sizes or distance, but to relative distance values ("greater than" or "less than"). The relative size of the intermediate area reflects the applicant's recognition of the advantage of the movement of air around the central area to provide further dissipation of heat.

Regarding claims 24, 26 and 28, Examiner acknowledges that Katchmar does not teach that the purpose of the smaller pitch of the central bumps is to allow them to melt together, but rather that Katchmar teaches a central heat transfer unitary body, as shown in the embodiment of Figure 4, made by applying a solder mass. However, Examiner argues that applicant's inclusion in the product claims of a method of making a unitary solder body using a plurality of solder balls with a determined pitch, cannot distinguish the application over the prior art. The Examiner cites as a well-settled rule that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product.

The product in this case, as the Examiner recognizes in paragraph 2 the Action, is a semiconductor device having a plurality of separate solder bumps disposed on the central area of a back surface of a substrate. No claim is made in the present application to a semiconductor device in which a solder mass is disposed in the central area of the back of the substrate. The rejected claims are not "product-by-process" claims, as the Examiner appears to be arguing. The limitation in question is directed to the criterion by which the spacing between the bumps in the central area is determined, rather than to any process

used in the manufacture of the semiconductor device. Although Katchmar discloses in Figure 5, for example, a semiconductor device having more closely spaced solder balls in the central area under the semiconductor chip, Katchmar fails to teach or suggest any criteria for selecting the distance between them, or that the distance should be advantageously selected so that they will fuse together to form a single mass during the reflow process used subsequently for mounting the semiconductor device.

Claim 28 is amended herein to remove a limitation that is not believed to be necessary for patentability. The limitation is now recited in new dependent claim 30. New claim 31 is added herein to provide greater protection for the invention disclosed in the application.

All objections and rejections having been addressed, it is respectfully submitted that the application is in condition for allowance, and notice of such, with allowed claims 20, 22 and 24-29, is earnestly solicited.

Respectfully submitted,

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Appendices 1 & 2

APPENDIX 1

AMENDMENTS TO CLAIMS

28. (Twice Amended) A semiconductor device, comprising:

a substrate having a main surface and a back surface, the back surface having a central area, an intermediate area surrounding the central area and a peripheral area surrounding the intermediate area;

a semiconductor chip disposed on the main surface;

a first bump unit disposed in the central area of the back surface to radiate heat from the semiconductor device, the first bump unit including a plurality of bumps disposed a first distance apart from each other; and

a second bump unit formed in the peripheral area of the back surface for transmitting signals, the second bump unit including a plurality of bumps disposed a second distance apart from each other sufficient to assure that upon application of a heat treatment to the device causing the bumps of the first and second bump units to melt, the bumps of the second bump unit remain apart from each other, the second distance being greater than the first distance; [and less than a third distance between the central area and the peripheral area,]

wherein the bumps of the first bump unit are sufficiently close to each other that upon the application of the heat treatment to the device, the bumps of the first bump unit fuse into a unitary body.

APPENDIX 2

AMENDMENTS TO SPECIFICATION

Amend the paragraph on page 4, lines 20-26, as follows:

As shown in Fig. 2, the radiation solder bumps 13 are located in the central region of the back surface of the substrate 11a. Surrounding the central region is an intermediate region in which no solder bumps are located. The connection solder bumps 14 are located in a peripheral region which surrounds the [central] intermediate region of the back surface of the substrate 11a. The connection solder bumps 14 are electrically connected to electrodes of the semiconductor chip through conductive lines formed in the substrate, respectively. Therefore the connection solder bumps 14 function as terminals for connecting the semiconductor device to an outside circuit.

Amend the paragraph on page 5, lines 10-15, as follows:

Since each of the connection solder bumps 14 is connected to one of the electrodes of the semiconductor chip, the connection solder bumps 14 should be connected to the connection pads 22 individually. Therefore, as shown in Figs. 1 and 2, the connections solder bumps are located with a predetermined pitch or distance so that the adjacent connection bumps 14 should not be joined together [each other] by the heat treatment (the joining of [pumps] bumps is called [as] a solder bridge). Figs. 1 and 2 also show that the width of the intermediate region is greater than the distance between the connection solder bumps 14.